ADVANCED OPTOELECTRONIC CIRCUITS: DETECTORS AND IMAGE SENSORS

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Keywords: CMOS, SPAD, time-resolved imaging, time-to-digital converter (TDC), time-correlated single-photon counting (TCSPC).

Contents

Summary

The focus of this chapter is advanced optoelectronic circuits, in particular optical detectors and imagers. Advanced optical techniques are presented involving the concept of time-resolved detection and images sensing, discussing pixels, architectures, and readout circuits in the context of performance trade-offs and application-specific solutions. A number of devices are discussed and their pros and cons are discussed in some detail vis-à-vis their implementation in CMOS VLSI processes. Sensor volume, power dissipation, and reliability are also important considerations in these designs.

We review the most important architectures available today in SPAD imagers and we discuss the architecture selection process in relation to the target application, so as to reduce supply and substrate noise while maintaining the overall performance of the sensor. We present and compare several sensors and we overview the results of one

such sensors implemented in an advanced deep-submicron CMOS technology and we propose improvements in sensing for optical microscopy, spectroscopy, and the medical imaging sciences.

1. Introduction

1.1. Photodetection Basics

Our story begins in 1839, when Edmond Becquerel discovers the photovoltaic effect and Willoughby Smith observes photoconductivity in selenium in 1873. In the last 140 years the field of optical detection has evolved from bulky single pixel devices to today's multi-megapixel fully integrated cameras. The improvements involved not only a resolution expansion but also the extension of spectral sensitivity and speed. With the emergence of the need of detecting individual photons, a useful feature in many applications involving photon counting, the invention of the photomultiplier tube (PMT) has become an important milestone that has enabled fundamental discoveries in physics, biology, chemistry, and the creation of revolutionary biomedical imaging devices responsible for today's advancement of medical sciences.

The 90-year-old PMT has not lost its usefulness but it is increasingly under pressure from solid-state devices capable of single-photon sensitivity with fewer constraints in terms of volume, power, and readout electronics. Among solid-state replacements of PMTs, the most notable device, known as silicon photomultiplier (SiPM), appeared in 2000[1]. A SiPM is essentially an array of avalanche photodiodes (APDs) operated in Geiger mode, whereas the individual avalanche currents are summed in one node and amplified. The main advantage of SiPMs is the relative simplicity of use and the fact that they are an almost perfect replacement of PMTs in terms of most performance measures. APDs operating in Geiger mode, known in the literature as single-photon avalanche diodes (SPADs) or Geiger-mode APDs (GAPDs), actually appeared before SiPMs with the seminal work of Cova et al. and McIntyre et al. in the 1980s [2], [3]. The peculiarity of SPADs is the fact that, unlike SiPMs, they enable to record the location where a photon has impinged. This functionality allows one to image a scene based on the source of the photons generated, reflected, or scattered by the objects in the scene.

1.2. Time-Correlated Single-Photon Counting

The detection of single photons is not relevant per se, while their time-of-arrival upon impingement is important in a number of applications. This mode of detection is known as time-correlated single-photon counting (TCSPC). With this feature, it is possible to reconstruct the properties of the object emitting or scattering the detected photons. Until recently, TCSPC could only be performed on a single spot of the sample with the use of a single pixel. To image the sample, it was necessary to scan the sample using electromechanical precision techniques.

With the emergence of miniature SPADs implemented in CMOS [4], [5]. first and multi-pixel SPAD arrays [6]. later, TCSPC could be potentially performed independently on each pixel. Nonetheless, the number of pixels was limited and the

time-of-arrival of photons required the use of external time-discriminators, usually time-to-digital converters (TDCs) or time-to-amplitude converters (TACs). It is only in 2008 that the first fully integrated imager was designed including a large array of SPADs and an array of TDCs on the same chip[7]. This work opened the way to the use of large-scale TCSPC at the pixel level thereby improving frame rate to video-speed and the instrument response function (IRF) of optical setups to sub-100-picoscond resolution [8].

1.3. Time-resolved Fluorescence Imaging

Thanks to the high time resolutions achieved in SPADs and SiPMs, it became possible to perform fluorescence detection in time- and spatially-resolved systems, whereas spatially one would use perhaps 2 or 4 independent single-pixel large sensors. In 2003 researchers could achieve fluorescence correlation spectroscopy (FCS) in more than one spot using a single integrated SPAD array[9]. SPADs could also be used for fluorescence lifetime imaging microscopy (FLIM) based on the TCSPC technique in two-photon regime on a single spot [8]. With the increase of the size of SPAD arrays, it became possible to image multi-spot systems, using a beamsplitter to create an array of highly focused illuminating points[10] . However, the number of spots in the systems is still limited by the power of the femtosecond laser source, since the power of each spot roughly halves by doubling of the number of spots.

To take advantage of the expanding number of pixels in SPAD arrays, along with an increasing time resolution of each SPAD-TDC pixel, one-photon FLIM techniques were used by several authors in combination with a wide-field microscope[11], [12],[13]. The main limitation of this approach is still given be a reduced fill factor due to the large surface occupied by the TDC in each pixel. This problem has been addressed with encouraging results with the use of microlens arrays [14]. The disadvantage of using conventional microlens arrays though is the relatively limited chief ray angle, that forces researchers to use collimated optical systems to take full advantage of the lenses. Current research focuses on a double approach of increasing the active area in pixel and of developing alternative micro-concentration devices.

1.4. Time-of-flight and 3D Imaging

Time-of-flight (TOF) imaging is another advanced sensing mode used in optical 3D imaging and rangefinding systems. The technique consists of applying TCSPC in combination with a laser source pulsed at high speed. The reflected photons are detected independently on the SPAD array and their time-of-arrival is measured with respect to the outgoing pulsed source. The time difference is the time required for the light to complete a round-trip from the source to the reflecting object.

The TOF can be computed independently on each pixel using an alternative method to TSCPC, known as single-photon synchronous detection (SPSD). The method consists of computing the phase between outgoing optical signals (modulated as a sinusoid) and the incoming light pulses. The phase difference may be computed by accumulating photon counted in 4 or more synchronous bins and by simple trigonometry operations on-pixel [15].

3D imaging and range finding are useful in a number of applications, where the relative position of two or more objects is sought, for example in automotive and aircraft collision avoidance systems, spacecraft docking, and security cameras. 3D imaging can also be used to build 3D profiles of objects in real time for cinematography, biometrics, entertainment, and games, where high-speed surface needs to have millimeter precision and megapixel resolution [7].

2. Detectors for Advanced Detectors and Imagers

2.1. Building CMOS Compatible Detectors

Building SiPMs and SPADs in CMOS substrates requires knowledge of the process and layers available to the designer to implement junctions that can be reverse-biased at high voltages Figure 1 shows a generic pn junction implemented in a planar process. The figure shows the depletion region, as it forms upon reverse biasing the junction (assuming a large doping differential between the p and n regions).
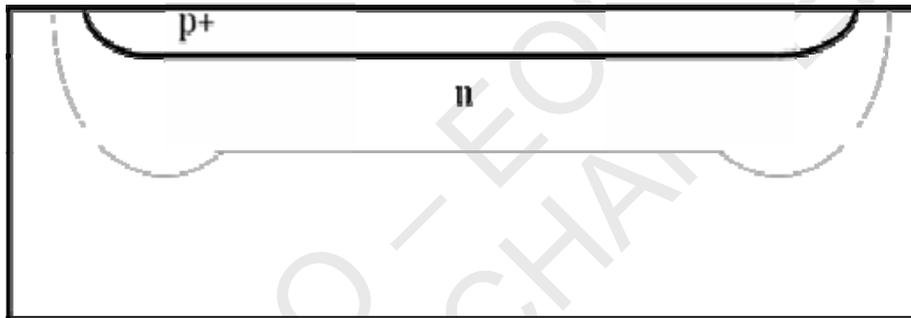

Figure 1. Cross-sections of a generic pn junction in a planar process with the depletion region (gray line) forming in the structure upon reverse-biasing, assuming a large doping differential between the p and n regions.

Implementing a pn junction in a planar process first involves finding a way to prevent premature edge breakdown (PEB). Several techniques exist to implement PEB prevention.

In essence, the techniques have in common the reduction of the electric field or the increase of the breakdown voltage at the edges of the junction, so as to maximize the probability that the avalanche is initiated in the center of the multiplication region, i.e. the region where the critical electric field for impact ionization is reached and, possibly, exceeded.

Figure 2 illustrates four of the most used structures. In a) the n+ layer maximizes the electric field in the middle of the diode. In b) the lightly doped p- implant reduces the electric field at the edge of the p+ implant. In c) a floating p implant locally increases the breakdown voltage at the edge. A polysilicon gate is usually drawn to prevent the creation of a shallow trench, however, it can also be used to further extend the depletion region.
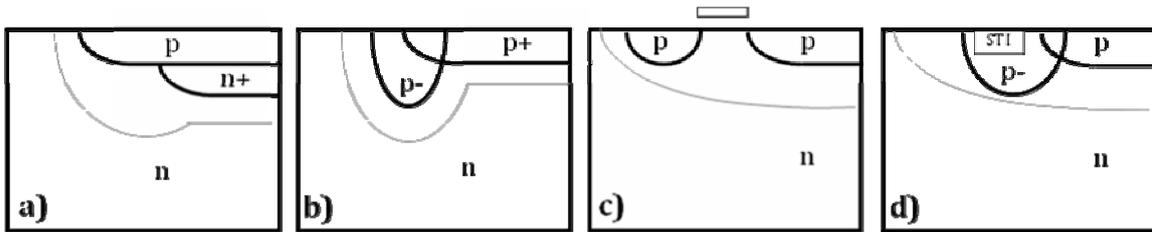
Figure 2. Cross-sections of doping profiles that may be used to prevent premature edge breakdown in planar processes.

Shallow trench isolation (STI) can also be used to delimit the junction, provided that it is surrounded by a multi-layer of doped silicon so as to force recombination of those charges generated in the defect-rich STI as shown in structure d) [17].

These structures are usually shaped as a ring around the junction; they are known as *guard rings*. Figure 3 depicts the distribution of the electric field across the junction in simulation.

The figure shows a field exceeding the critical value required to cause impact ionization at room temperature in the center of the junction. A sub-critical field can be seen in correspondence of the guard ring and in a planar zone known as inactive space [17].
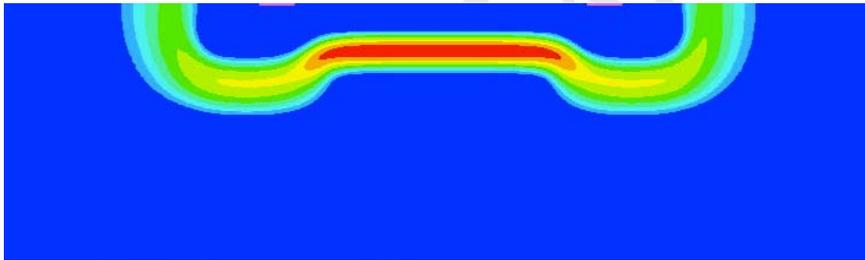

Figure 3. Distribution of the electric field under the pn junction and the guard ring. Electric field exceeds critical for a sustained avalanche in the center of the pn junction, a region commonly referred to as multiplication region.

The impact ionization process is well understood and the literature on the subject is extensive [18]. When impact ionization occurs, for example due to electron-hole pair photo- or thermal generation, an avalanche may be initiated, thus enabling inherent amplification of the original event. When a pn junction is biased above breakdown, the optical gain becomes infinite.

In this regime, known as Geiger mode of operation, the pn junction may break down, due to avalanche generation. Upon occurrence of an avalanche, destruction of the device is prevented by a quenching mechanism, whose sole function is to rapidly quench the avalanche.

Upon avalanche quenching, there is a period of recharge, used to relax the device, i.e. to allow the primary avalanche process to come to an end, and to ready it for the next photon detection [19]. The photon detection process is divided into four distinct states:

- *idle state*, the initial state in which the device must be in order to detect the next photon;
- *buildup*, the process of creation and reinforcement of the avalanche;
- *spread* and *quenching*, the avalanche expansion and its end;
- *recharge*, the recovery from the avalanche and the preparation to return to the idle state.

Collectively known as dead time, these states are sequentially reached, usually requiring from a minimum of 6ns in the most advanced active quenching/recharge implementations [20]. to a maximum of a few microseconds, in the older discrete SPAD implementations.

2.2. Working with CMOS Processes: Biasing, Quenching, and Recharge

In the remainder of the chapter we focus our attention to schemes (b) and (d), because they require, in general no modifications to the process and thus enable the design of large SPAD array chips in standard CMOS technologies.

There exist a variety of avalanche quenching techniques, partitioned in active and passive methods. The literature on these variants is extensive [21]. In active methods, the avalanche is detected and stopped by acting on the bias. In passive methods the pn junction bias is self-adjusted e.g. by a ballast resistor. Recharge methods can also be active and passive. In active methods, the bias across the diode is re-established by a switch activated by an avalanche detector. In passive methods the recharge occurs through the ballast.
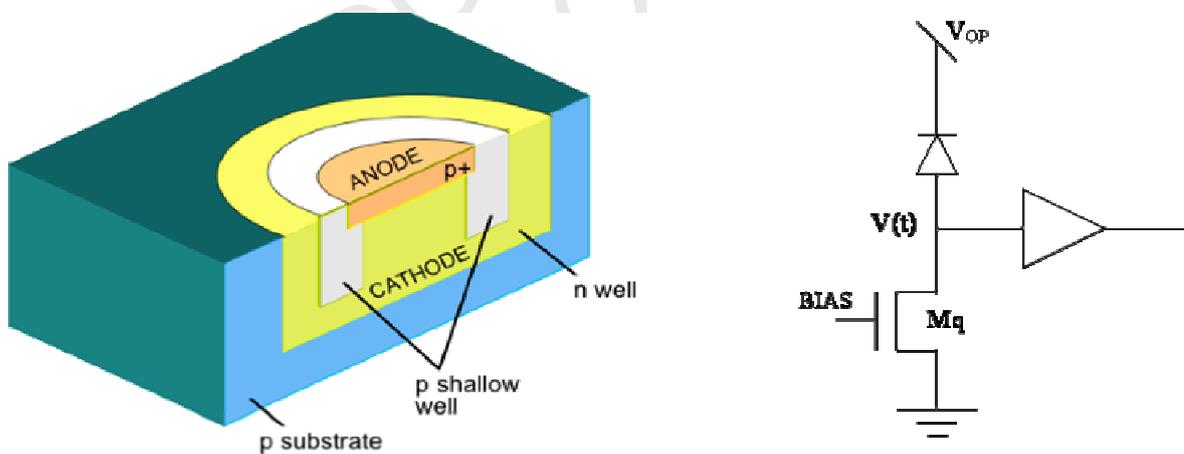
Figure 4. SPAD cross-section in a CMOS process (left); passive quench and recharge circuitries, as well as pulse shaping (right).

Figure 4 shows the cross-section of a SPAD and simple circuitry to perform passive quench and recharge. Upon photon detection, the device generates a current pulse that is converted to a digital voltage level by means of a pulse shaping circuitry, also shown in the figure. The pulse shaper is also acting as an impedance adapter to drive the load of

the column readout often employed in a SPAD matrix. The ballast may be implemented as a resistor or as an active element acting as a non-linear resistor (M_q in Figure 4).

By proper selection of bias, one can operate in active quenching and active recharge mode, where I_R is the current discharged by M_q of Figure 4. In reality, the transistor may not be operated in strong inversion throughout the recharge and thus the linear discharge is only an approximation.

The advantage of using an active recharge is a better control of the dead time. Furthermore, active recharge can also be performed in multi-slope mode to allow for a precise control of dead time over larger SPAD arrays, thus improving overall detection uniformity, especially in high illumination regimes.

Figure 5 shows three typical recharge profiles. Passive recharge is the most commonly used technique, while active recharge is used in many devices whereby the recharge process has to respond to specific requirements. Figure 5 also shows two types of active recharge known as single- and double-slope active recharge. Single-slope recharge is simple to implement requiring only one bias per SPAD.

In double-slope recharge [15], the SPAD's dead time is effectively controlled by time t_R at which the second slope is activated. If the voltage V_R achieved at this point still disables the avalanche, then it is guaranteed that the device is still in dead time regime. Thus the dead time can be triggered by one properly timed control signal and thus it is independent of R .
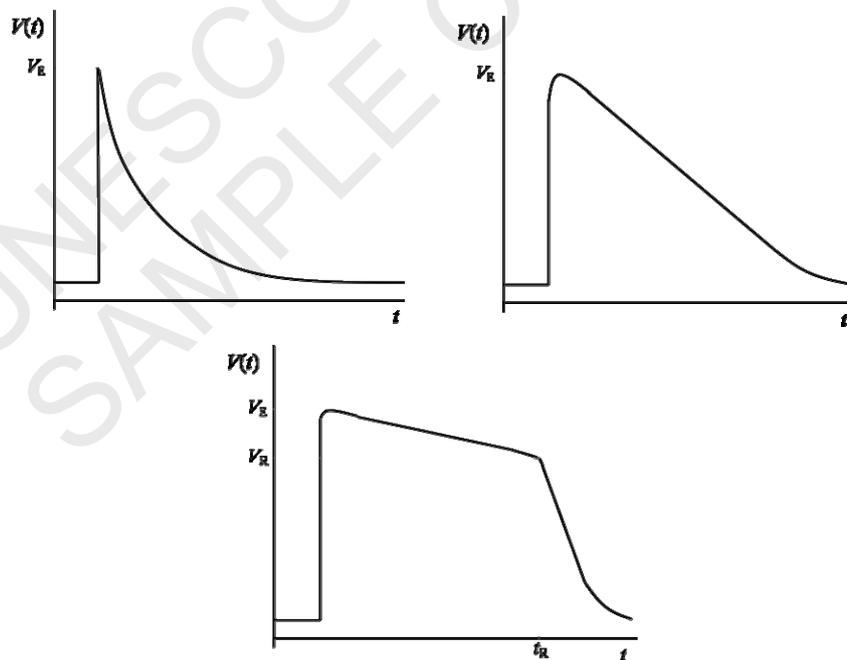

Figure 5. SPAD recharge mechanisms: passive (left), single-slope active (center), and double-slope active (right).

A wide variety of quenching and recharge circuits can be found in the literature whereby the differentiating factors are complexity.

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Biography Sketch

Edoardo Charbon received the Diploma from ETH Zurich in 1988, the M.S. degree from UCSD in 1991, and the Ph.D. degree from UC-Berkeley in 1995, all in Electrical Engineering and EECS. From 1995 to 2000, he was with Cadence Design Systems, where he was the architect of the company's initiative on information hiding for intellectual property protection. In 2000, he joined Canesta Inc. as its Chief Architect, leading the development of wireless 3-D CMOS image sensors. Canesta was sold to Microsoft in 2010. Since November 2002, he has been a member of the Faculty of EPFL in Lausanne, Switzerland, working in the field of CMOS sensors, biophotonics, and ultra low-power wireless embedded systems. In Fall 2008 he has joined the Faculty of TU Delft, as full professor in VLSI design, succeeding Patrick Dewilde. Dr. Charbon has consulted for numerous organizations, including Texas

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